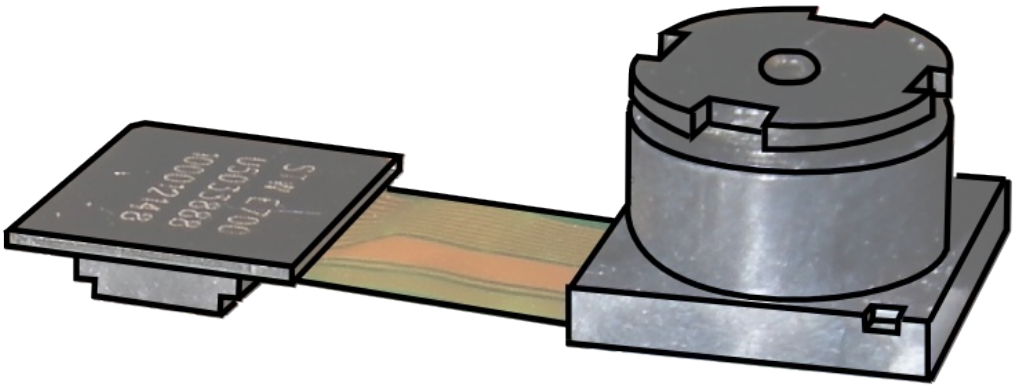
SparkFun Camera Manual

P/N: Sense-CCAM



Revision 0.1b, Aug 14, 2006

Overview

The Spark Fun SENSE-CCAM camera is a 640x480 [vga resolution] camera with an 8 bit digital interface. The camera is based on a Hynix/MagnaChip HV7131GP. This document does not attempt serve as a replacement for the HV7131GP datasheet, especially with regards to its register set. This document is intended to familiarize new users to the camera, and provide information not covered in the datasheet such as the camera package / pinout, along with things the author discovered the hard way.

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1. Pinout / Connections

The connector of the CCAM is a 20 pin receptacle on an 0.4mm pitch. Specific part number is DF18C-20DS-0.4V. This connector mates with part # DF18C-20DP-0.4V.

Pinout:

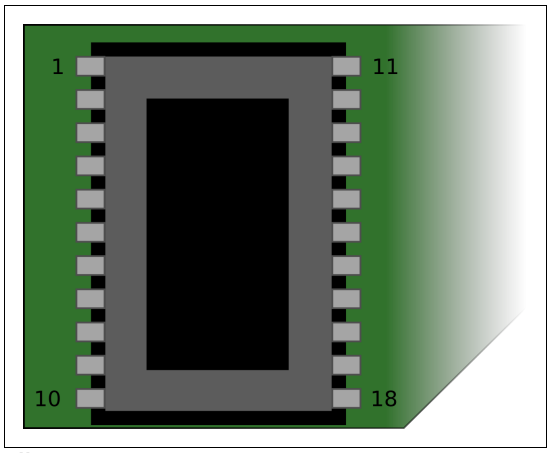


Illustration 1: Connector pinout [as seen looking at connector flex from backside of camera].

Pin	*Description*		*Pin*	*Description*
1	Y0 [out]	Data Bus	11	ENB [in] – Enable Camera
2	Y1 [out]		12	/RST [in] – Reset Camera
3	Y2 [out]		13	GND
4	Y3 [out]		14	VCC
5	Y4 [out]		15	SCL [inout] – I2C Clock
6	Y5 [out]		16	SDA [inout] – I2C Data
7	Y6 [out]		17	Vsync [out] – Vertical Sync
8	Y7 [out]		18	Hsync [out] – Horizontal Sync
9	VCC		19	PCLK [out] – Pixel Clock
10	GND		20	CLK_in [in] – Clock Input

2. Electrical / Signalling

2.1 Power Supply / IO Voltages

Recommended VCC: 2.8-3.0V

Maximum VCC for proper operation: 3.2V

Output Voltages [Observed]: 0 - VCC

Input Voltages: 0-VCC [3.3V Signalling directly in seems to work fine with VCC = 3.0]

2.2 Standard Frame Waveform

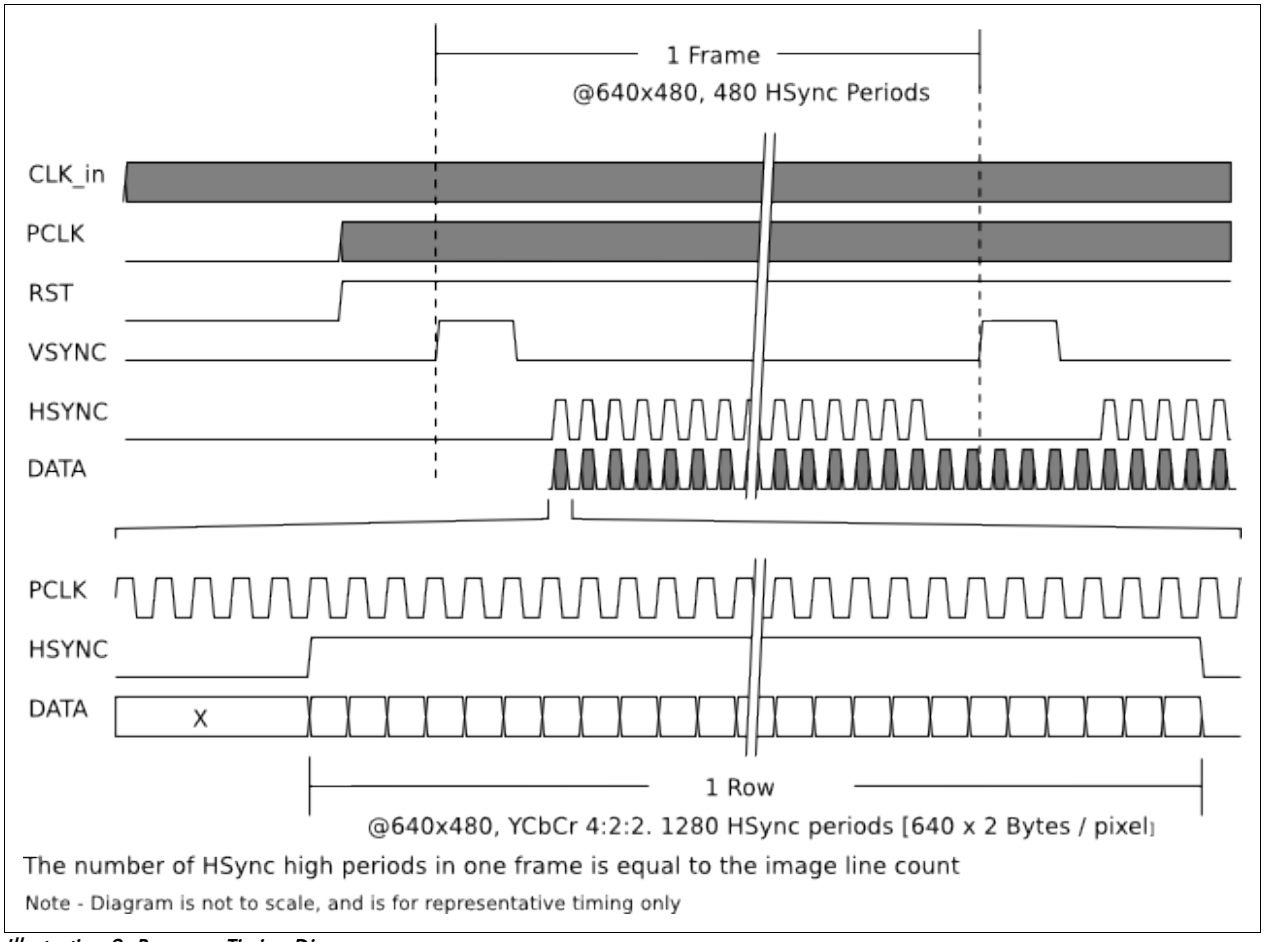


Illustration 2: Powerup Timing Diagram

A single byte of data is clocked on every pclk pulse. See data formats section for the interpretation of this data. PCLK and CLK_in are NOT necessarily in phase or the same frequency. The phase shift seems to be dependant on the frequency supplied to CLK_in. The frequency may be divided depending on the settings set via I2C.

HSYNC / DATA should be read on every negative edge of PCLK [this is hard to do with a micro]. DATA is only valid while HSYNC is high.

A frame consists of all the bytes of data while HSYNC is high, between a falling and a rising edge of VSYNC.

2.3 Data Formats

The camera supports multiple data formats, the default of which is 4:2:2 YcbCr.

YCbCr is a format which encodes color as the luminance of the color [how bright it is], and Cb and Cr which jointly indicate the hue of color.

I use the following code [constants taken from the imager datasheet] to convert YCbCr to RGB. Parameters provided are Y Cb and Cr in the range 0 to 0xFF, and it calculates r g and b bytes in the range of 0 to 0xFF. This code can be considerably improved, especially by using a fixed point routine, but that is at the expense of readability.

```
uint8_t Y,Cb,Cr;

float calcR = Y + 1.371f * (Cr - 128);
float calcG = Y - 0.698f * (Cr - 128) - 0.336 * (Cb - 128);
float calcB = Y + 1.732f * (Cb - 128);

if (calcR < 0) calcR = 0;
if (calcG < 0) calcG = 0;
if (calcB < 0) calcB = 0;

uint8_t r_byte = ((int)calcR) & 0xFF;
uint8_t g_byte = ((int)calcG) & 0xFF;
uint8_t b_byte = ((int)calcB) & 0xFF;
```

The 4:2:2 notation indicates that for every 4 luminance values provided, you get 2 Cb, and 2 Cr. The reason for this is that the human eye is much more sensitive towards Luminance than it is to color variations, so you don't notice much of a quality loss if you use the same Cb/Cr for two pixels.

In the default mode, data is transmitted in the following order:

Y0, Cb0, Y1, Cr1, Y2, Cb2, Y3, Cb3 and so on....

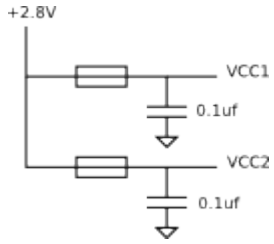
To calculate the RGB constant of pixel 1, you would use Y0, Cb0, and Cr1. For the second pixel, Y1 Cb0 and Cr1. The same pattern repeats for the rest of the image, providing 4 bytes of data for each 2 pixels.

2.4 Camera PCB design and Layout

Unlike some lower speed electronics, the CCAM connector / peripheral circuitry needs to be laid out following proper SI practices to obtain a clean signal. A ground plane is highly recommended, thus requiring at least a 2 layer pcb.

Clk_in, PCLK, HSYNC, VSYNC at minimum should all be routed over a continuous, uninterrupted ground plane. Guard traces/bands are recommended, especially for long runs. [A guard band is essentially a strip of gnd in between two traces to decrease crosstalk].

As the camera has an analog portion that is very sensitive to noise and power supply fluctuations, decoupling is mandatory, and filtering with a ferrite bead is highly recommended. [One bead per VDD, as one is analog and one is digital]. I recommend an 0.1uf capacitor, and a ferrite bead rated at at least 30ma, with parameters of something like 600ohms @ 100mhz



3. Example Application

4. Mechanical Form Factor