Delay Line for Analogue Signals

Monolithic integrated circuit in MOS technology for the delay of analogue signals in the frequency range up to 250 kHz. It ist designed according to the principle of the bucket circuit and comprises 185 series-connected field effect transistors and 185 integrated capacitors.

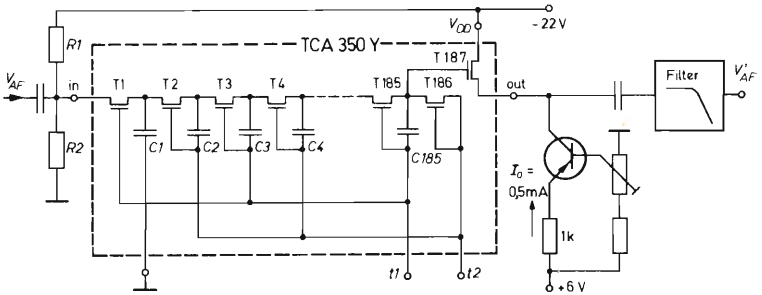
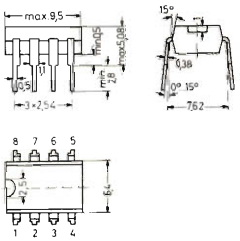


Fig. 1: Internal circuitry and test circuit of the TCA 350 Y with external components

Fig. 2:
TCA 350 Y in plastic package
20 A 8 according to DIN 41 866

Weight approx. 0.5 g
Dimensions in mm



Pin connections

1 Leave vacant
2 Clock input *t2*
3 Delay line input
4 Ground, 0
5 Clock input *t1*
6 Delay line output
7 V_{DD}
8 NC

All voltages are referred to ground (pin 4)

Maximum Ratings

Drain voltage	V_{DD}	− 30 . . . + 0.3	V
Input voltage	V_{in}	− 30 . . . + 0.3	V
Clock pulse voltages	V_{t1}, V_{t2}	− 30 . . . + 0.3	V
Output current	I_o	− 5	mA
Storage temperature range	T_S	− 40 . . . + 100	°C

Recommended Operating Conditions

Drain voltage	V_{DD}	− 22 (− 20 . . . − 24)	V
Clock pulse voltage (see Fig. 7) high state	V_{tH}	− 1 . . . + 0.3	V
low state	V_{tL}	− 18 (− 17.5 . . . − 20)	V
Clock frequency (see Fig. 5) when $f_t > 2\, f_{AFmax}$	$f_t = \frac{1}{T_t}$	40 (10 . . . 500)	kHz
Clock pulse duration	t_1, t_2	> 0.8	µs
Interval between two clock pulses	t_{1p}, t_{2p}	> 0 (not overlapping)	
Signal pulse duty factor (see Fig. 8)	$\frac{t_1 + t_{1p}}{T_t}$	0.1 . . . 0.9 [1]	
Rise and fall time of the clock pulses	t_r, t_f	0.05 . . . 10	µs
Input bias voltage	V_{in}	− 8 (− 7.5 . . . − 8.5)	V
Impedance of bias source at the input	$\frac{R_1 \cdot R_2}{R_1 + R_2}$	< 20	kΩ
Input signal amplitude (peak-to-peak, see Fig. 10)	V_{AFpp}	3 (0 . . . 6)	V
Input impedance of the filter at output	R_{inF}	> 20	kΩ
Output DC current (current of the constant current source see Fig. 11)	I_o	0.5 . . . 1.5 [2]	mA
Ambient operating temp. range	T_{amb}	− 20 . . . + 60	°C

[1]) The output signal is proportional $\frac{t_1 + t_{1p}}{T}$, because during the time $t_1 + t_{1p}$ the AF signal appears at the output.

[2]) If the filter input impedance R_{IF} exceeds 1 MΩ, the constant current source at the output may be replaced by a resistor $R_L > 10$ kΩ (see Fig. 12).

Characteristics

at $V_{DD} = -22$ V, $V_{in} = -8$ V, $V_{AFpp} = 6$ V, $f_{AF} = 400$ Hz, $V_{tH} = 0$, $V_{tL} = -18$ V, $f_t = 40$ kHz, $t_1/T_t = t_2/T_t = 0.48$, $t_r = t_f = 2$ µs, $I_o = 0.5$ mA, $T_{amb} = 25$ °C in the circuit Fig. 1 which includes the Butterworth filter at the output. The latter has a cutoff frequency of 8 kHz, an input impedance of 43 kΩ and an attenuation of 110 dB at kHz. These test conditions apply equally to Figs. 3 . . . 12.

Delay time ($\tau = \frac{184}{2 \cdot f_t}$)	τ	2.3	ms
Attenuation [1])	a	8.5 (< 10)	dB
Distortion factor	k	0.5 (< 3)	%
Noise voltage, peak-to-peak (see Fig. 6)	V_{Npp}	1.2 (< 2)	mV
Noise voltage, RMS value (see Fig. 6)	$V_{N\,RMS}$	0.2 (< 0.35)	mV
Clock input capacitances	C_t	150	pF

[1]) In the test circuit the AF signal appears at the output only for the duration $t_1 + t_{1D} = T/2$. This amounts to a 6 dB attenuation. Only the residual 2.5 . . . 4 dB of the above quoted attenuation can be ascribed to the delay line.

Design and Operation Mode

Fig. 1 shows the circuit diagram of the TCA 350 Y and the external circuit components.

The output transistor T 187 requires a drain voltage of − 22 V from which the necessary input bias of − 8 V is produced by a potential divider. Connected to the source terminal of the output transistor T 187, which operates as a source follower, is a 0.5 mA constant current source which acts as a load resistance and caters for voltage variations from + 5 V to − 22 V at the output of the TCA 350 Y. This ensures distortion-free transmission of the two bands of the output signal (see Fig. 3).

Fig. 4 illustrates the time relationship between clock signal and output signal as scaled by the clock frequency. The information contained in the output signal appears during the onset of clock pulse t_1 and is maintained up to the onset of clock pulse t_2. During t_1 the input information is scanned, i. e. the capacitor *C1* absorbs the information via the turned-on transistor T1. Every subsequent clock pulse (t_1 as well as t_2) shifts this information into the next capacitor of the chain. With the 185th pulse (of which 93 pulses are t_1 and 92 pulses t_2) the information reaches the last capacitor of the chain, i. e. *C185*, and, after amplification, becomes available via the source-follower T187 at the output of the TCA 350 Y. As is apparent from Fig. 4, the information is preserved up to the onset of t_2, although the signal voltage is raised by about 14 V after the expiry of t_1.

In this way the lower signal band is produced during t_1, and the upper signal band during t_{1p}. Which proportion of the intelligence is contained in the lower, and which in the upper signal band depends upon the ratio of the clock pulse duration t_1 to the clock pulse interval t_{1p}. Thus, if $t_{1p} = 0$ information is transmitted exclusively in the lower signal band.

The delay time of the bucket brigade circuit TCA 350 Y is calculated by using the following equation:

$$\tau = \frac{n}{2 \cdot f_t} = \frac{184}{2 \cdot f_t}$$

wherein n is the number of buckets in the chain (in the present case 184 because capacitor *C1* does not contribute to the delay time).

The lowpass connected to the output of the TCA 350 Y filters the delayed signal V'_{AF} from the output signal of the TCA 350 Y which contains the clock voltage.

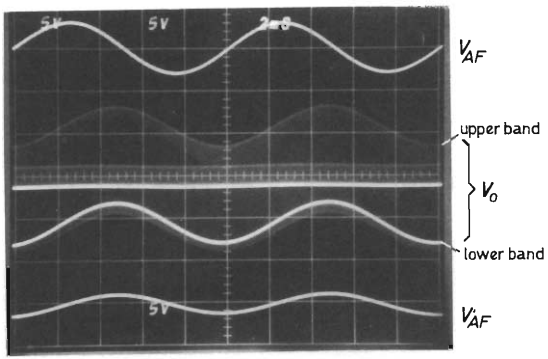


Fig. 3: Input and output voltages of the circuit shown in Fig. 1

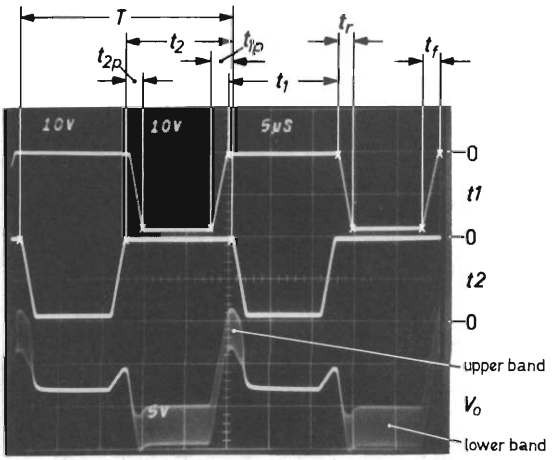


Fig. 4: Output voltage and clock voltages of the circuit shown in Fig. 1

Fig. 5:
Distortion factor
versus clock frequency

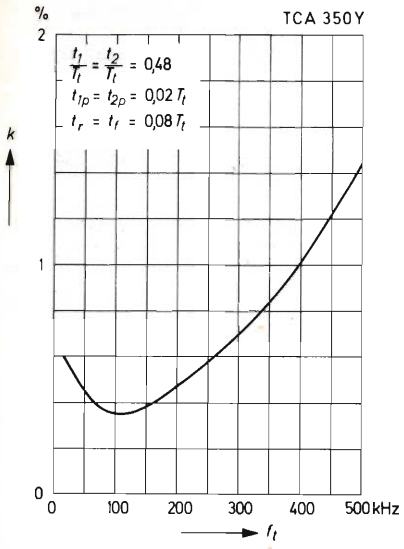


Fig. 6:
Noise voltage
versus clock frequency

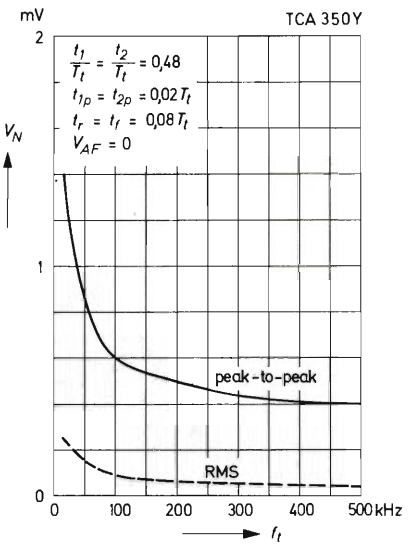


Fig. 7:
Distortion factor
versus clock amplitude

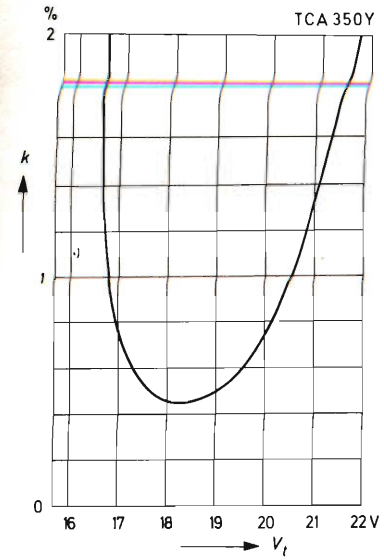


Fig. 8:
Distortion factor versus
pulse duty factor of the
clock signal

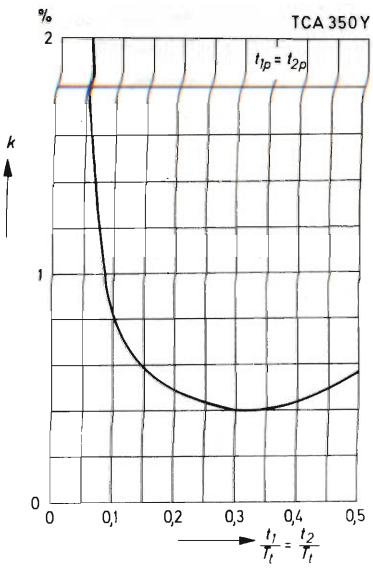


Fig. 9:
Distortion factor versus signal pulse duty factor

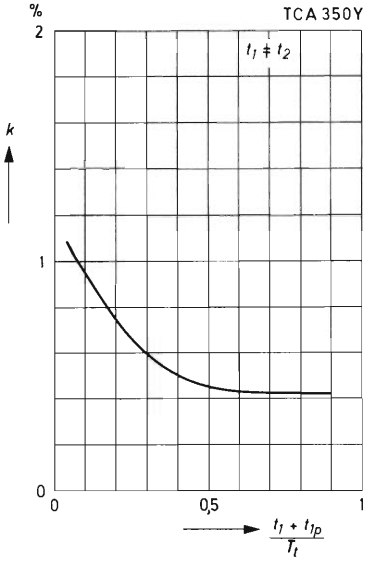


Fig. 10:
Distortion factor versus signal amplitude at input

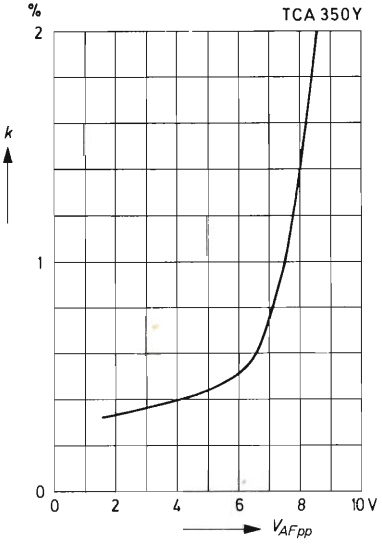


Fig. 11:
Distortion factor versus current of constant current source

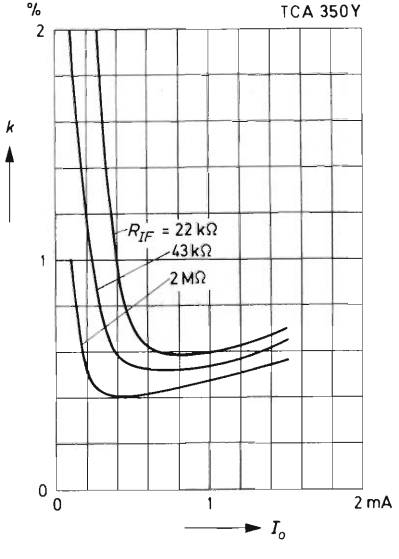


Fig. 12:
Distortion factor versus ohmic load resistance at output