TECHNICAL DATA

AN EXCLUSIVE RADIO SHACK SERVICE TO THE EXPERIMENTER

SAD-1024 DUAL ANALOG DELAY LINE

DESCRIPTION:

The SAD-1024 is a general-purpose dual 512-stage Bucket-Brigade Device (BBD) fabricated using N-channel silicon-gate technology to obtain flexible performance at low cost. Each 512-stage section is independent as to input, output, and clock. The sections may be used independently, may be multiplexed to give an increased effective sample rate, may be connected in series to give increased delay, or may be operated in a differential mode for reduced even-harmonic distortion and reduced clocking noise. Each section has its output split into two channels so that in normal operation output is provided over each full clock period. The SAD-1024 is packaged in a standard 16-lead dual-in-line package. Only V_{dd} and GND are common to the two separate delay sections.

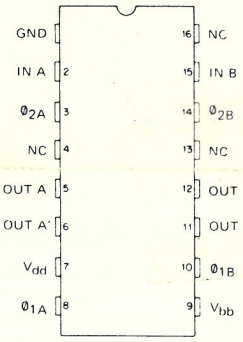


Figure 1. Pin Configuration, SAD-1024. Note: Unused outputs should be connected to V_{dd}; all other unused pins should be connected to GND (pin 1), including those marked N.C.

KEY FEATURES:

- Two independent 512-stage delay sections.
- Clock-controlled delay: 0.5 sec to less than 200μsec.
- N-channel silicon-gate bucket-brigade technology.
- Designed for self-cancellation of clocking modulation.
- Wide signal-frequency range: 0 to more than 200kHz.
- Wide sampling clock frequency range: 1.5kHz to more than 1.5MHz.
- Wide dynamic range: S/N >70db.
- Low distortion: less than 1%.
- Low noise: typically limited by output amplifier.
- Single 15 volt power supply.

TYPICAL APPLICATIONS:

- Voice control of tape recorders.
- Variable signal control of amplitude or of equalization filters.
- Reverberation effects in stereo equipment.
- Tremolo, vibrato, or chorus effects in electronic musical instruments.
- Variable or fixed delay of analog signals.
- Time compression of telephone conversations or other analog signals.
- Voice scrambling systems.

DEVICE CHARACTERISTICS AND OPERATING PARAMETERS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Clock Voltage[1]	ϕ_1 ϕ_2	10	15	17	Volts
Drain Supply Voltage[1]	V_{dd}	10	15	17	Volts
Bias Voltage[1]	V_{bb}		V_{dd}-1	V_{dd}	Volts
Sampling Freq.	$f\phi_1$, $f\phi_2$	0.0015	—	1.5	MHz
Clock Rise Time	t_{cr}		30		nsec
Clock Fall Time	t_{cf}		50		nsec
Clock Line Capacitance	C_c		110		pf
Signal Freq. Bandwidth (3db point)		See Fig. 2	200		kHz
Gain[2]			1.2		
Input Capacitance	C_{in}		7		pf
Input Shunt Resistance[3]	R_{in}			200	Kohms
Optimum Input Bias[4]			+6		Volts
Maximum Input Signal Amplitude		1	2		Volts p-p
Average Temp. Coefficient of Gain[6]			—.01		db/°C
Average Temp. Coefficient of Optimum Input Bias[6]			.8		mv/°C

Notes:

1. All voltages measured with respect to GND (pin 1).
2. The value of gain depends on the output termination resistance. See Figure 4.
3. Effective a-c shunt resistance measured at 1MHz.
4. The input bias voltage varies slightly with the magnitude of the clock voltage (and V_{dd}) and may be adjusted for optimum linearity at maximum signal level. The value shown is nominal for 15 volt clocks.
5. The device may be operated at clock voltages down to 5 volts (to facilitate use in battery operated portable equipment) but with reduced input bias and reduced input signal amplitude.
6. Measured at sample frequency of 10kHz, audio input of 1V p-p at 1kHz in SC-1024A circuit for temperature range of 0° to 70°C.

ABSOLUTE MAXIMUM VOLTAGES

TERMINAL	LIMITS	UNITS
Any terminal[1]	+20 to —0.4	Volts

CAUTION:
Static discharge to any lead of this device may cause permanent damage. Store in aluminum foil or inserted in conductive foam. Use grounded soldering irons, tools, and personnel when handling devices. Avoid synthetic fabrics. It is recommended that the device be inserted into socket before applying power.

SUMMARY OF OPERATION

The SAD-1024 is an analog-sampled data device which lies between linear and digital in it's applications and method of use. The input data is handled in analog form in discrete time, controlled by an external clock. Internally, the data is handled in samples at fixed intervals, much as in any digital system. The input analog signal is connected to the first of the 512 MOS transistors while the clock frequency is high and is transmitted to the next section when the clock goes low. The amplitude of the input signal remains constant between sections. The clock signals appear at the output as part of the "mix" and must be filtered out.

DRIVE AND VOLTAGE REQUIREMENTS

Voltage levels and limits are given in the specifications table on page 1. The clock inputs are two-phase square waves. For convenience in use, $V_{bb}=V_{dd}$. However, for optimum performance, V_{bb} should be one volt less than V_{dd}. All unused outputs should be connected to V_{dd}. All unused terminals (including the ones marked NC) should be connected to ground. The bandwidth of the input should be limited to less than one-half of the clock frequency.

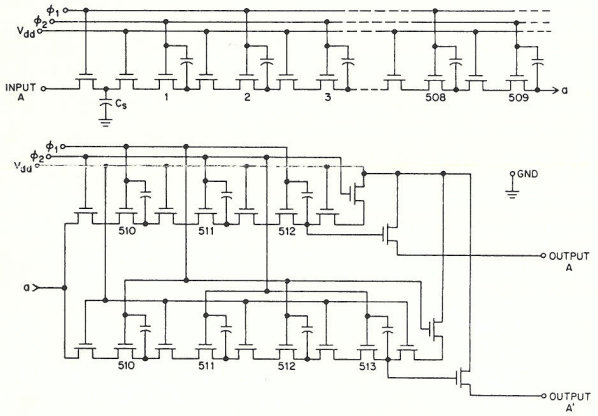


Figure 2. Equivalent Circuit Diagram for One Section SAD-1024

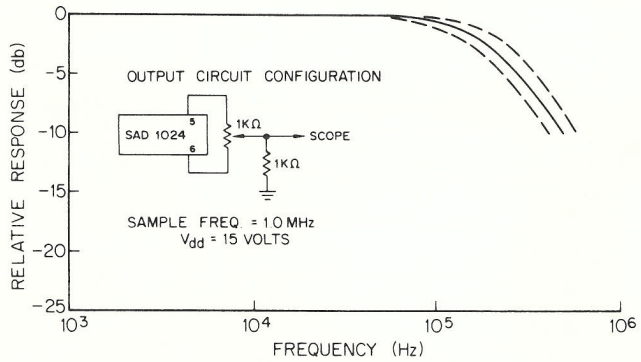


Figure 3. Frequency Response showing Typical Variation Device to Device.

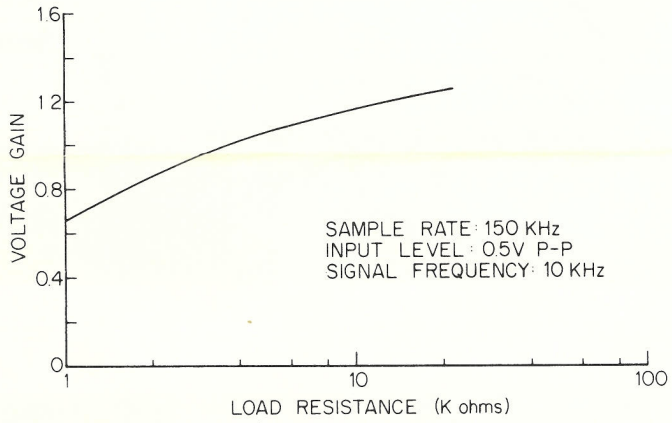


Figure 4. Dependence of Gain on Load Resistance.

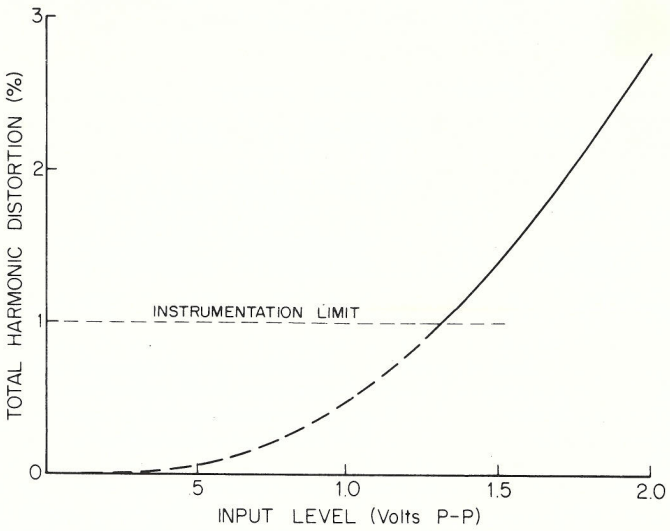


Figure 5. SAD-1024 Distortion vs. Input Level.

CLOCKING

Schematics for two types of variable-frequency clock generators are shown in Figure 6. Both are easy-to-build and provide a wide range of clock frequencies.

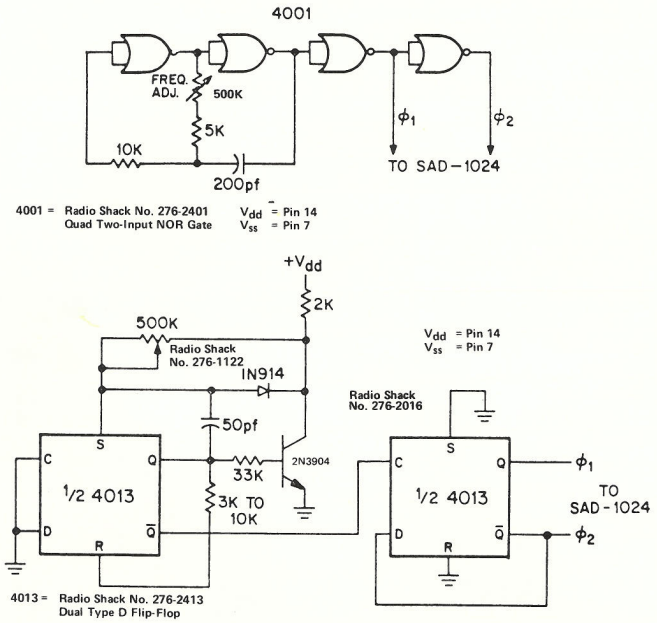


Figure 6. Two Examples of a Simple Variable-Frequency Clock Generator.

CIRCUIT CONFIGURATIONS

The SAD-1024 consists of two 512—element delay sections which, except for common grounds and power input, are electrically independent. The sections may be used in the following configurations:

1. Single-section
2. Serial
3. Parallel-multiplex
4. Differential
5. Multiple-device

1. Normal single-section configuration

In this configuration, the A and B sections are completely independent. Different inputs and different clocks can be used for each section. The outputs at A and A' (likewise B and B') must be externally summed as shown in Figure 7.

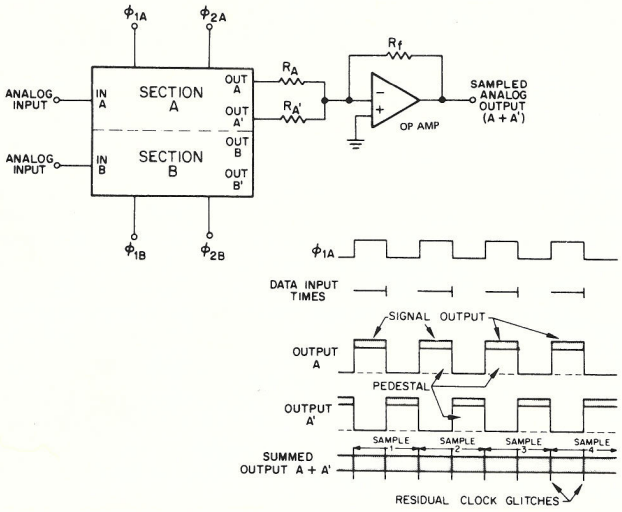


Figure 7. Single-Section Operation. Connect unused outputs to V_{dd} and all other unused pins to ground.

2. Serial configuration

By using the output of section A as the input of section B, this configuration doubles the delay time. As shown in Figure 8, the output from section A must be slightly attenuated so the input level to section B equals the original input level.

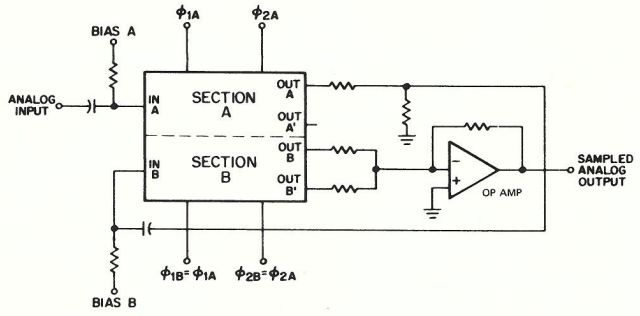


Figure 8. Serial Connection of Delay Sections. Waveforms are entirely similar to those for single-section operation. Connect unused outputs to V_{dd}.

3. Parallel-multiplex operation

This configuration doubles the number of samples for the same delay or doubles the delay for the same clock rate. Superior performance results when the clock frequency is held constant and the delay doubled, causing the individual sections of the BBD to operate at one-half the system rate. This configuration is best for use at clock frequencies above 200 kHz. If the clock frequency is lower, serial operation is preferred.

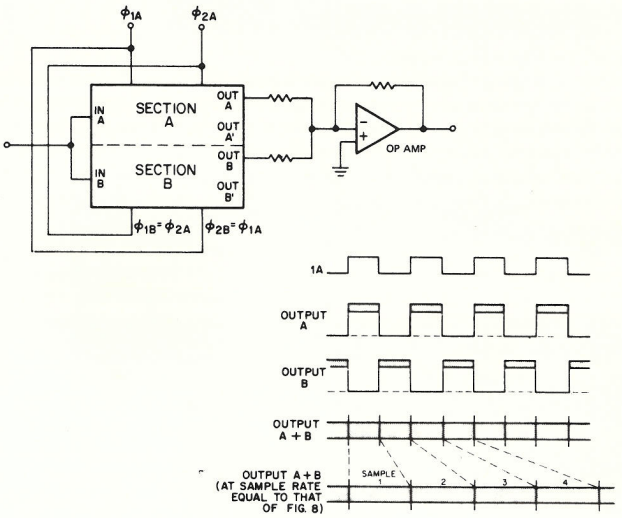


Figure 9. Parallel-Multiplex Operation. Connect unused outputs to V_{dd}.

4. Differential operation

In this configuration, clocking glitches are more effectively cancelled. This configuration also results in the cancellation of even harmonics. (See Figure 10.) The operation of the BBD is similar to the single-section configuration.

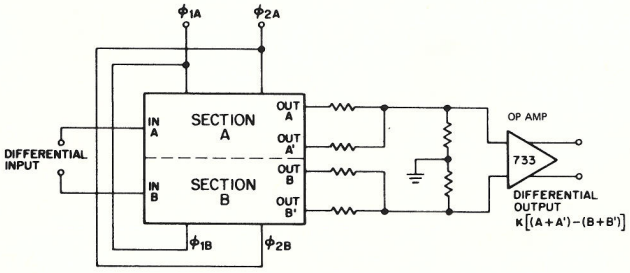


Figure 10. Differential Operation

5. Multiple-device operation

When multiple SAD-1024 chips are connected together, any of the configurations described above can be used. In the serial configuration, gain must be restored between sections. Since the gain of each section is slightly more than one, a resistance network can be used between sections.

When using multiple chips in the parallel-multiple configuration, the phase of the clock must be shifted to each successive device by π/N radians (N=number of chips).

NOTES ON OPERATION

For the best performance, remember that the SAD-1024 has important input and output requirements. To avoid distortion, the bandwidth of the input signal must be filtered to less than half of the clock frequency. (Filtering to one-third of the clock frequency is preferred to provide a guard band.) Clocking "glitches" also appear at the outputs as high-frequency components and should be removed by a low-pass filter with a cutoff at about half the clock frequency.

For non-critical applications, a simple output circuit as shown in Figure 11 can be used. For the best performance, high-quality summing operational amplifiers should be used for output filtering.

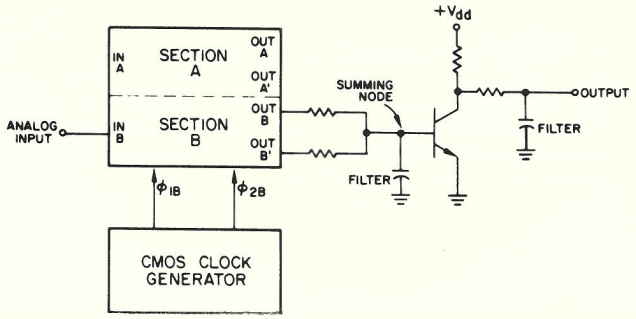
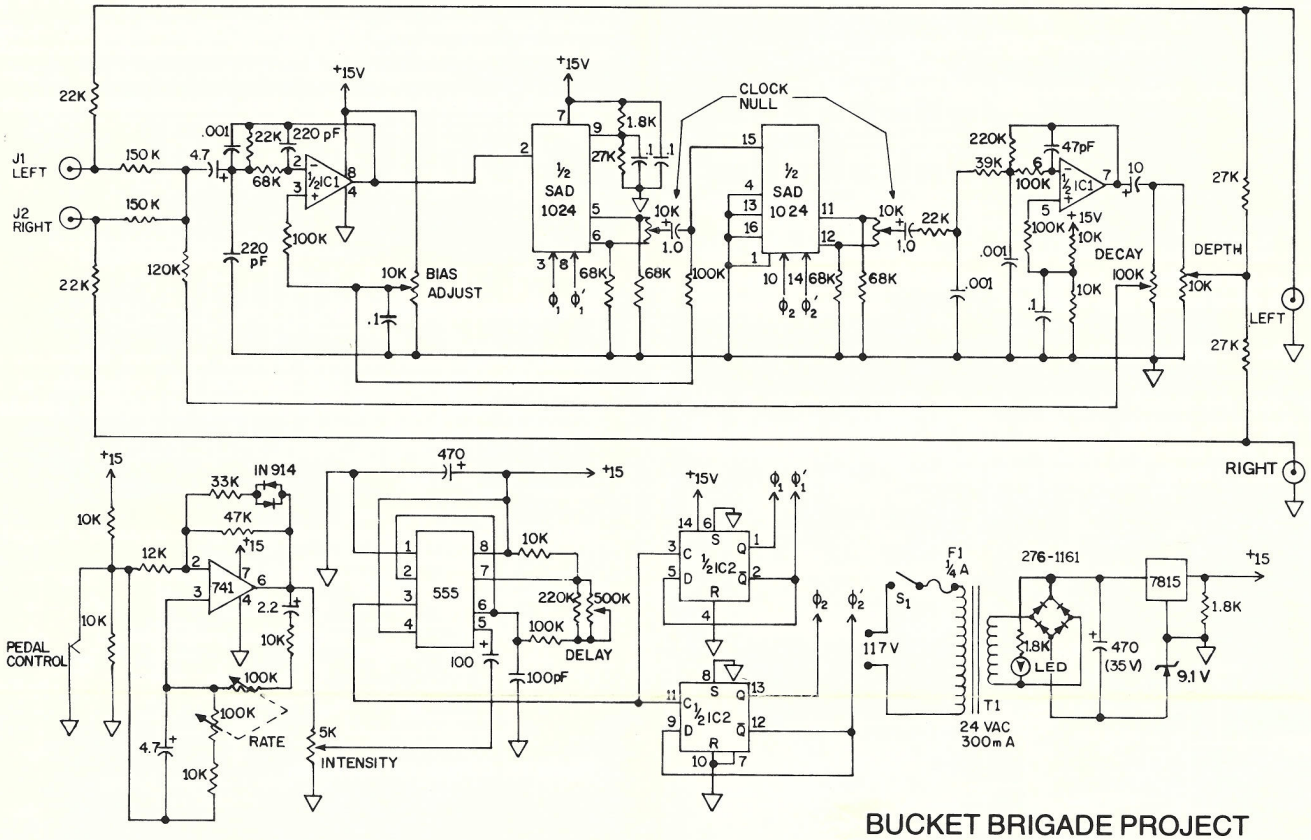


Figure 11. Simple Output Summing Amplifier. Connect unused outputs to V_{dd} and all other unused pins to ground.



BUCKET BRIGADE PROJECT

IC1 1458 8PINS
IC2 4013 14 PINS
SAD 1024 16 PINS
741 8PINS
555 8PINS

RADIO SHACK A DIVISION OF TANDY CORPORATION

U.S.A.: FORT WORTH, TEXAS 76102
CANADA: BARRIE, ONTARIO L4M 4W5

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AUSTRALIA	BELGIUM	U. K.
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